said collectors of said power semiconductor elements are pressed by said plate-like collector electrode terminal so that said collectors and said collector electrode terminal are electrically connected together, and

said main emitters of said power semiconductor elements are pressed by said plate-like emitter electrode terminal so that said main emitters and said emitter electrode terminal are electrically connected together.

REMARKS

Favorable reconsideration of this application is respectfully requested.

Claims 23-32 are pending for examination in this application. Claims 23, 25, 27, 29, and 31 have been amended to better clarify the nature of the gate(s) as being arranged on the now recited channel(s) between the collector(s) and main emitter(s) and to emphasize that the potential of the gate(s) is controlled according to electrical current flow passing through the current sense terminal, all without the introduction of any new matter.

The outstanding Office Action mailed September 19, 2002, presents a rejection of Claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa et al (U.S. Patent No. 5,874,750, Yanagisawa), and a rejection of Claims 24-32 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa in view of Takeda et al (1998 International Symposium article, Takeda).

Before considering the outstanding prior art rejections applied to Claims 23-32, it is believed that a brief summary of the invention thereof would be helpful. In this regard, the present invention involves a chip-like voltage-driven power semiconductor element with at least one insulated gate and power semiconductor device including this element. The element has a collector formed on one side and the insulated gate and main emitter formed

on the other side thereof along with a current sense terminal. Current flow is from the collector to both the main emitter and the current sense terminal and potential on the gate is controlled according to electric current passing through the current sense terminal. Note the explanation of benefits in the specification at page 60, lines 3-12 and page 60, line 26-page 61, line 7, for example.

The present invention is further concerned with the element being an injection enhanced gate transistor (IEGT) and providing for operating with an electron injection efficiency at the main emitter and the current sense terminal of 0.73 or more. Note the explanation of benefits and properties in the specification at page 72, line 21 through page 73, line 26, for example, with particular regard to page 73, lines 21-26 and FIGS. 46 and 47 as to electron ejection efficiency.

Turning to the rejection of Claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Yanagisawa, it is noted that Claims 23 require an injection enhanced gate transistor (IEGT) that has a gate that is "arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said gate." Thus, the Claim 23 recited IEGT clearly has MOS-type structure in which a gate is formed on a channel region with a gate insulating film interposed between the gate and the channel region, where this MOS-type IEGT is also recited to have an electron injection efficiency at the main emitter and the current sense terminal that is 0.73 or more.

The outstanding Action errs in suggesting that the limitation of the electron injection efficiency being 0.73 can be dismissed as being an optimum value of a result effective variable, the discovery of which involves only routine skill. However, the conventional IGBT structure adopted by Yanagisawa would have a problem if the electron injection efficiency is provided as 0.73 or more because the injection efficiency would be too high at

the emitter. This would prevent the gate voltage from controlling the switching operation between the collector and emitter.

The outstanding Action attempts to suggest that the Yanagisawa IGBT structure is the same as that of a standard NPN bipolar transistor (at page 5) and would have an electron efficiency of 0.73 or more. However, a standard NPN bipolar transistor performs as an electric current driven transistor that controls the current between the emitter and collector with a base current and can have an electron injection efficiency that is 0.73 or more. On the other hand, an injection enhanced gate transistor (IEGT) like that of Claim 23, is of MOS-type and has a gate formed on a channel region with a gate insulating film interposed between the gate and the channel region so as to be a voltage driven transistor that controls the current between the emitter and the collector through the gate potential.

Clearly, if the Yanagisawa IGBT structure is the same as that of a standard NPN bipolar transistor (as argued at page 5 of the outstanding Action), then it would have the above-noted standard current control and not be readable as the Claim 23 injection enhanced gate transistor (IEGT) that must be of MOS-type and have a gate formed on a channel region with a gate insulating film interposed between the gate and the channel region so as to be a voltage driven transistor that controls the current between the emitter and the collector through the gate potential.

Accordingly, if the PTO maintains its second position that the IGBT relied on from Yanagisawa has the same structure as a standard NPN bipolar transistor (as argued at page 5 of the outstanding Action) to inherently have an electron injection efficiency that is 0.73 or more, then it cannot be said to be readable as the Claim 23 injection enhanced gate transistor (IEGT) that must be of MOS-type and have a gate formed on a channel region with a gate insulating film interposed between the gate and the channel region so as to be a voltage

driven transistor that controls the current between the emitter and the collector through the gate potential. Thus, the rejection should be withdrawn.

On the other hand, if the PTO maintains its first position that the IGBT relied on from Yanagisawa has the same structure as the injection enhanced gate transistor (IEGT) that must be of MOS-type and have a gate formed on a channel region with a gate insulating film interposed between the gate and the channel region so as to be a voltage driven transistor that controls the current between the emitter and the collector through the gate potential, then the electron injection efficiency that is 0.73 or more cannot be said to be inherent as with a standard NPN current driven transistor.

Moreover, in this second case, the fact that there is problem as to operating an injection enhanced gate transistor (IEGT) of MOS-type with the Claim 23 recited electron injection efficiency that is 0.73 or more cannot be ignored any more than the cure offered by the presently claimed IGET can be ignored. See FIG. 47 again and note the IGBT curve there for an IGBET like that of Yanagisawa and the IEGT curve illustrated therein. Thus, it is clear that the electron injection efficiency at the main emitter being 0.73 or greater cannot be considered as an optimum value at which Yanagisawa's IGBET device could operate and such an efficiency cannot be derived from Yanagisawa or considered to be obvious over this reference.

In this last regard, it is well established that the rule of In re Boesch, cited at the bottom of page 2 of the outstanding Office Action, is not a rule implying that optimization to achieve results not disclosed by the prior art is "obvious." See In re Antonie, 195 USPQ 6, 8-9 (CCPA 1977) as follows:

> The PTO and the minority appear to argue that it would always be obvious for one of ordinary skill in the art to try varying every parameter of a system in order to optimize the effectiveness of the system even if there is no evidence in the record that the prior art recognized that particular parameter

affected the result. As we have said many times, obvious to try is not the standard of 35 USC § 103. *In re Tomlinson*, 53 CCPA 14231, 363 F.2d 928, 150 USPQ 623 (1966). Disregard for the unobviousness of the results of "obvious to try" experiments disregards the "invention as a whole" concept of § 103, *In re Dien*, 54 CCPA 1027, 371 F.2d 886, 152 USPQ 550 (1967) and *In re Wiggins*, 55 CCPA 1356, 397 F.2d 356, 158 USPQ 199 (1968), and overemphasis on the routine nature of the data gathering required to arrive at appellant's discovery, after its existence became expected, overlooks the last sentence of § 103. *In re Saether*, 492 F.2d 849, 181 USPQ 36 (CCPA 1974). [Footnote omitted.]

In *In re Aller*, 42 CCPA 824, 220 F.2d 454, 105 USPQ 233 (1955), the court set out the rule that the discovery of an optimum value of a variable in a known process is normally obvious. We have found exceptions to this rule in cases where the results of optimizing a variable, which was known to be result effective, were unexpectedly good. *In re Waymouth*, 499 F.2d 1273, 182 USPQ 290 (CCPA 1974); *In re Saether, supra*. This case, in which the parameter optimized was not recognized to be a result-effective variable, is another exception. The decision of the board is reversed. [Emphasis added.]

As further noted in the last response:

The court in Antonie further noted (at 195 USPQ 8) that the consideration of the invention as a whole requires consideration of claimed values such as the electron injection efficiency value of 0.73 claimed here and the inherent properties of the invention claimed as follows:

> In determining whether the invention as a whole would have been obvious under 35 U.S.C. § 103, we must first delineate the invention as a whole. In delineating the invention as a whole, we look not only to the subject matter which is literally recited in the claim in question (the ratio value) but also to those properties of the subject matter which are inherent in the subject matter and are disclosed in the specification. *In re Davies*, 475 F.2d 667, 177 USPQ 381 (CCPA 1973). In this case, the invention as a whole is the [claimed] value . . . and its inherent and disclosed property.
>
> * * *
>
> The controlling question is simply whether the differences (namely the [claimed] value . . . and its property) between the prior art and appellant's invention as a whole are such that appellant's invention as whole would have been obvious.

This is the controlling question here as well. The anser to this controlling question is clearly that Yanagisawa does not teach or reasonably

suggest the differences here as to the claimed "current sense terminal" or the claimed "electron injection efficiency at said main emitter and said current sense terminal" that "is 0.73 or more," much less the inherent properties associated therewith. Accordingly, it is believed to be clear that Claim 23 and its delineated invention considered as a whole have not been shown to be *prima facie* obvious. Thus, this rejection of Claim 23 is traversed.

Claim 24 depends on Claim 23 and includes all the limitations thereof. Moreover, nothing fairly taught or reasonably suggested by Takeda cures the deficiencies noted above as to Yanagisawa. Therefore, the rejection of Claim 24 is traversed for the reasons noted above as to Claim 23. In addition, Claim 24 adds further features not reasonably taught by Yanagisawa and/or Takeda taken alone or together in any reasonable combination and the rejection of Claim 24 is traversed for this reason as well.

With further regard to Claims 25, 26, and 28, even though these claims do not depend on Claim 23, they do include the relevant limitations of an "electron injection efficiency" as "being 0.73 or more" and the Claim 23 requirement for an injection enhanced gate transistor (IEGT) that must be of MOS-type and have a gate formed on a channel region with a gate insulating film interposed between the gate and the channel region so as to be a voltage driven transistor that controls the current between the emitter and the collector through the gate potential Thus, as Takeda cures none of the deficiencies noted above as to Yanagisawa and to these limitations, Claims 25, 26, and 28 are also believed to patentably define over these references for the reasons noted above as to Claim 23.

Furthermore, all of Claims 23-32 require a current sense terminal and controlling potential on at least one gate according to an electric current passing through this current sense terminal. The outstanding Action appears to suggest (in the paragraph bridging pages 4 and 5) that it is reasonable to read the Yanagisawa voltage sense emitter that detects the voltage on the emitter electrode as this current sense terminal of Yanagisawa based on an Ohm's law relationship of current flow through a resistor being related to voltage (I=V/R).

However, this is an overly simplistic analogy as a potential can exist at the emitter electrode and be measured there with no current flow. Thus, the detection of 0V on the emitter electrode cannot be converted to a current using Ohm's law. Moreover, the presence of this zero volt potential, or any other potential detected by the voltage sense emitter of Yanagisawa, is not taught to be used to control the potential on the gate as all of these claims require.

Once again, Takeda cures none of the deficiencies noted above as to Yanagisawa such that Claims 23-32 that recite the "current sense terminal" and associated control of the potential on the gate voltage should be considered to be allowable thereover.

As it is believed that no other issues remain outstanding in this application, it is further believed that this application is, accordingly, in condition for formal allowance and an early and favorable action to that effect is, therefore, respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

Please amend Claims 23, 25, 27, 29, and 31 as follows:

--23. (Twice Amended) An injection enhanced gate transistor (IEGT) made of a semiconductor chip, comprising:

a collector formed on one side of said semiconductor chip;

a main emitter formed on an opposing side of the semiconductor chip that opposes said one side of the semiconductor chip;

a gate formed on [an] said opposing side [which opposes said one side] of the semiconductor chip, said gate being arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said gate; and

[a main emitter formed on said opposing side of the semiconductor chip; and]

a current sense terminal formed on said opposing side of the semiconductor chip, a potential of said gate being controlled according to an electric current passing through said current sense terminal,

wherein electrical current from said collector is made to flow to both said main emitter and said current sense terminal, and

electron injection efficiency at said main emitter and said current sense terminal is 0.73 or more.

25. (Twice Amended) A voltage-driven power semiconductor device, comprising:

a chip-like injection enhanced gate transistor (IEGT) having a collector on one side, and further having a main emitter, a current sense terminal, and a gate on an opposing side which opposes said one side, said gate being arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said gate, a potential of said gate being controlled according to an electric current passing through said current sense terminal, electrical current from said collector being made to flow to both said main emitter and said current sense terminal, and electron injection efficiency at said main emitter and said current sense terminal being 0.73 or more;

a plate-like collector electrode terminal arranged on said one side of said IEGT and electrically connected to said collector; and

a plate-like emitter electrode terminal arranged on said opposing side of said IEGT and electrically connected to said main emitter,

wherein said voltage-driven power semiconductor device is a press-contacting type package,

said collector of said power semiconductor device is pressed by said plate-like collector electrode terminal so that said collector and said collector electrode terminal are electrically connected together, and

said main emitter of said power semiconductor device is pressed by said plate-like emitter electrode terminal so that said main emitter and said emitter electrode terminal are electrically connected together.

27. (Twice Amended) A voltage-driven power semiconductor device, comprising:

a chip-like voltage-driven power semiconductor element having a collector on one side, a main emitter, a current sense terminal, and a gate on an opposing side which opposes

said one side, said gate being arranged on a channel region between said collector and said main emitter with a gate insulating film interposed between said channel region and said gate, a potential of said gate being controlled according to an electric current passing through said current sense terminal, and electrical current from said collector being made to flow to both said main emitter and said current sense terminal;

a plate-like collector electrode terminal arranged on said one side of said power semiconductor device and electrically connected to said collector; and

a plate-like emitter electrode terminal arranged on said opposing side of said power semiconductor device and electrically connected to said main emitter,

wherein said voltage-driven power semiconductor device is a press-contacting type package,

said collector of said power semiconductor device is pressed by said plate-like collector electrode terminal so that said collector and said collector electrode terminal are electrically connected together, and

said main emitter of said power semiconductor device is pressed by said plate-like emitter electrode terminal so that said main emitter and said emitter electrode terminal are electrically connected together.

29. (Twice Amended) A voltage-driven power semiconductor device, comprising:

a plurality of voltage-driven power semiconductor elements connected in series and in parallel, said power semiconductor elements including semiconductor chips and said semiconductor chips having collectors on one side, and main emitters, at least one current sense terminal, and gates on an opposing side which opposes said one side, said gates being arranged on a channel regions between said collectors and said main emitters with gate insulating films interposed between said channel regions and said gates, potential of said

gates being controlled according to an electric current passing through said current sense terminal, and electrical current from said collectors being made to flow to both said main emitters and said at least one current sense terminal;

a plate-like collector electrode terminal arranged on said one side of said plurality of power semiconductor elements, and electrically connected to said collectors; and

a plate-like emitter electrode terminal arranged on said opposing side of said plurality of power semiconductor elements and electrically connected to said main emitters,

wherein said voltage-driven power semiconductor device is a press-contacting type package,

said collectors of said power semiconductor elements are pressed by said plate-like collector electrode terminal so that said collectors and said collector electrode terminal are electrically connected together, and

said main emitters of said power semiconductor elements are pressed by said plate-like emitter electrode terminal so that said main emitters and said emitter electrode terminal are electrically connected together.

31. (Amended) A voltage-driven power semiconductor device comprising:

a plurality of voltage-driven power semiconductor elements connected in series and in parallel, said power semiconductor elements including semiconductor chips and said semiconductor chips having collectors on one side, and main emitters, at least one current sense terminal, and gates on an opposing side which opposes said one side, said gates being arranged on a channel regions between said collectors and said main emitters with gate insulating films interposed between said channel regions and said gates, potential of said gates being controlled according to an electric current passing through said current sense terminal, electrical current from said collectors being made to flow to both said main emitters

and said at least one current sense terminal, and said gates being a trench-type gate embedded in said opposing side;

a plate-like collector electrode terminal arranged on said one side of said plurality of power semiconductor elements, and electrically connected to said collectors; and

a plate-like emitter electrode terminal arranged on said opposing side of said plurality of power semiconductor elements and electrically connected to said main emitters;

wherein said voltage-driven power semiconductor device is a press-contacting type package,

said collectors of said power semiconductor elements are pressed by said plate-like collector electrode terminal so that said collectors and said collector electrode terminal are electrically connected together, and

said main emitters of said power semiconductor elements are pressed by said plate-like emitter electrode terminal so that said main emitters and said emitter electrode terminal are electrically connected together.--